

## CLAIMS

What is claimed is:

1. A method for forming a semiconductor device assembly, comprising:  
providing a carrier substrate including at least one die-attach location and at least one terminal adjacent to said at least one die-attach location; and  
providing a solder mask on said carrier substrate, said solder mask including at least one device-securing region positioned over at least a portion of said at least one die-attach location, at least one recessed area adjacent to said at least one device-securing region, and at least one dam adjacent to said at least one recessed area, opposite from said at least one device-securing region, said at least one dam contacting at least a portion of a peripheral edge of said at least one terminal.
2. The method of claim 1, further comprising:  
applying adhesive material to at least one of said at least one device-securing region of said solder mask and a bottom surface of at least one semiconductor device to be secured to said at least one device-securing region.
3. The method of claim 2, further comprising:  
positioning said at least one semiconductor device to said at least one device-securing region, said adhesive material located between said bottom surface and said at least one device-securing region securing said at least one semiconductor device to said at least one device-securing region.
4. The method of claim 3, wherein said positioning comprises applying force to at least one of said at least one semiconductor device and said carrier substrate.
5. The method of claim 3, wherein said positioning comprises forcing said adhesive material to spread between said bottom surface of said at least one semiconductor device and said at least one device-securing region.

6. The method of claim 5, wherein said positioning comprises causing excess adhesive material to flow laterally beyond at least one of a peripheral edge of said at least one semiconductor device and a periphery of said at least one device-securing region.

7. The method of claim 6, further comprising:  
receiving said excess adhesive material within said at least one recessed area.

8. The method of claim 6, wherein said at least one dam prevents said excess adhesive material from contaminating a connection surface of said at least one terminal.

9. The method of claim 1, wherein said providing said solder mask comprises providing a solder mask with said at least one dam comprising a laterally extending portion configured to cover at least portion of a peripheral edge of a connection surface of said at least one terminal.

10. The method of claim 1, wherein said providing said solder mask comprises providing said carrier substrate with said solder mask already secured thereto.

11. The method of claim 1, wherein said providing said solder mask includes securing a preformed solder mask to a surface of said carrier substrate.

12. The method of claim 1, wherein said providing said solder mask includes forming said solder mask on a surface of said carrier substrate.

13. The method of claim 12, wherein said forming is effected stereolithographically.

14. The method of claim 12, wherein said forming comprises forming a plurality of at least partially superimposed, contiguous, mutually adhered material layers.

15. A method for a designing solder mask for use on a carrier substrate, comprising:  
configuring at least one device-securing region to have a semiconductor device secured thereto;  
and  
configuring a plurality of raised dams to be positioned adjacent to and in contact with peripheries  
of terminals of the carrier substrate.

16. The method of claim 15, further comprising:  
configuring at least one recessed area between at least a portion of a periphery of said at least one  
device-securing region and at least one of said plurality of raised dams.

17. A method for designing a solder mask for use on a carrier substrate, comprising:  
configuring at least one device-securing region to have a semiconductor device secured thereto;  
and  
configuring at least one recessed area adjacent to said at least one device-securing region.

18. The method of claim 17, further comprising:  
configuring a plurality of raised dams adjacent to said at least one recessed area, opposite from  
said at least one device-securing region.

19. A method for designing a solder mask to be used on a carrier substrate,  
comprising:  
configuring at least one device-securing region of the solder mask to be located over at least a  
portion of a die-attach location of the carrier substrate;  
configuring at least one recessed area laterally adjacent to said at least one device-securing  
region; and  
configuring at least one dam adjacent to said at least one recessed area, opposite from said at  
least one device-securing region, to be located laterally adjacent to and contact a  
peripheral edge of a terminal protruding from a surface of the carrier substrate, and to  
have a height at least as great as a height of said at least one device-securing region.

20. The method of claim 19, wherein said configuring said at least one dam comprises configuring said at least one dam to include a laterally extending ledge positionable over at least a portion of a peripheral edge of a connection surface of the terminal.

21. The method of claim 19, wherein said configuring said at least one dam comprises configuring said at least one dam to have a height that exceeds said height of said at least one device-securing region.

22. The method of claim 21, wherein said configuring said at least one dam comprises configuring said at least one dam to be located at an elevation which is substantially the same as or less than an elevation of an active surface of a semiconductor device to be positioned on said at least one device-securing region.

23. A method for designing a carrier substrate, comprising:  
configuring a substantially planar substrate to include at least one die-attach location; and  
configuring at least one terminal adjacent to said at least one die-attach location and to protrude a sufficient distance from said substantially planar substrate to prevent excess adhesive material forced from between a semiconductor device and said at least one die-attach location from contaminating a connection surface of said at least one terminal.

24. The method of claim 23, further comprising:  
configuring an adhesive-receiving area between said at least one die-attach location and said at least one terminal.

25. The method of claim 24, wherein said configuring said adhesive-receiving area comprises configuring at least one recess.

26. The method of claim 25, wherein said configuring at least one recess comprises configuring said at least one recess to substantially laterally surround said at least one die-attach location.

27. The method of claim 25, wherein said configuring at least one recess comprises configuring said at least one recess to be located adjacent to only a portion of said at least one die-attach location.

28. The method of claim 23, wherein said configuring said at least one terminal comprises configuring said at least one terminal to have a height that is at least as great as an elevation at which a bottom surface of the semiconductor device will be supported above a surface of said substantially planar substrate.

29. The method of claim 28, wherein said configuring said at least one terminal comprises configuring said at least one terminal to have a height that is, at most, substantially the same as an elevation at which a top surface of the semiconductor device will be located upon securing the semiconductor device relative to said substantially planar substrate.